REMARKS

Applicant respectfully traverses and requests reconsideration.

Applicant wishes to thank the Examiner for the notice that claim 5 would be allowable if written in independent form. New claim 25 has been added which includes subject matter indicated to be allowable.

Claim 1 has been objected to due to a typographical error. The typographical error has been corrected.

Claims 1-4 and 6-24 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,774,131 (Kim) in view of Dutton. This is a new ground of rejection. The Kim reference is directed to a sound generation and display control apparatus for personal digital assistants that utilizes control logic 150 for interfacing between the central processing unit and the bus arbitrator and memory controller 14. An address generator 153 generates an address for an apparatus which displays graphics data under control of the control logic, a sound engine generates sound data in accordance with control of the control logic and the control logic outputs the address of the apparatus which outputs a sound corresponding to the sound data, among other things. (Col. 4, lns. 1-19). In operation as best understood, either the graphics engine 151 is selected via selection signal SLT by the CPU via the control logic to operate, or the sound engine 156 is selected to generate an echo, mix a sound, convert text into speech and output corresponding data to the data FIFO circuit 155. Accordingly, the control logic 150 is separate from and different from the bus arbitrator and memory controller 14 as specifically described by Kim and as shown in the figures. The bus arbitrator and memory controller 14 actually arbitrates "the allocations of the system bus for controlling the access to and refreshment of the memory 12" (col. 3, lns. 51-55). The control logic 150 does not perform

any bus arbitration nor does it provide incoming data from a local bus to the audio processing circuit or the video processing circuit. In fact, as stated in the Kim reference, a select (SLT) signal is actually sent by the central processing unit 11 to control the control logic 150 to select between the graphics processing engine and the sound engine 156. (See col. 4, lns. 36-55; see also FIG. 3). As shown in FIG. 2, the bus arbitrator 14 in Kim is connected to the control logic via graphic bus request and graphic bus acknowledge signals.

Claim 1 requires, inter alia, a local bus operative to receive incoming data from the system bus and is also operatively coupled to the graphics processing circuit and the audio processing circuit. The office action alleges that Kim teaches such a local bus as the "bus coupled to the control logic 150 from the graphics engine 151 and sound engine 156 inside coprocessor 15" (office action, page 3). However, the claim also requires that the local bus is coupled to a bus arbitrator. However, Applicant is unable to find an internal bus inside the coprocessor that is coupled from the graphics engine and sound engine to control logic 150 that also receives incoming data from a system bus. The only bus arbitrator in Kim is the bus arbitrator and memory controller 14.

The claim also requires the bus arbitrator is coupled to the local bus and to the graphics processing circuit and audio processing circuit wherein the arbitrator interprets the incoming data from the local bus and provides the incoming data from the local bus to the audio processing circuit or the video processing circuit based on the interpretation of the incoming data. The office action alleges that the claimed bus arbitrator is control logic 150. However, Applicant respectfully submits that the words "bus arbitrator" as actually used by Kim and are used to reference block 14, not block 150 since block 150 is control logic and is not a bus arbitrator. The bus arbitrator 14 in Kim does not interpret incoming data from the local bus or provide incoming

data to the audio processing circuit or the graphics processing circuit via a local bus. To the contrary, the bus arbitrator and memory controller 14 in the Kim reference is "for arbitrating the allocations of the system bus and for controlling the access to and refreshment of [system] memory 12" (col. 3, lns. 54-56).

As noted above, the control logic 150 is not a bus arbitrator as alleged since the bus arbitrator described in Kim is actually block 14. Accordingly, the reference does not teach what is alleged. Therefore, the claims are in condition for allowance.

In addition, or alternatively, control logic 150 also does not interpret the incoming data from the local bus and provide the incoming data to the audio processing circuit or the video graphics processing circuit wherein the incoming data was from a system bus as required in the claim. The control logic instead utilizes a SLT or select input to tell the control logic to operate the graphics engine or operate the sound engine. There is no need for the control logic 150 to interpret the incoming data as received by a local bus from a system bus and provide the incoming data to either the audio processing circuit or the video processing circuit after the interpretation of the incoming data. Instead, the select input SLT from the CPU for the control logic 150 forces the control logic 150 to control either the graphics engine or the sound engine. (See for example, col. 4, lns. 40-45).

Although the claim is allowable for any one of the above reasons, Applicant also respectfully notes that the office action admits that Kim fails to teach that the bus arbitrator arbitrates outputting data on the local bus from the graphics processing circuit and the audio processing circuit after it has interpreted the incoming data from the local bus that was received from the system bus. Dutton has been cited as allegedly teaching this subject matter. However, Dutton teaches a different structure and operation. The bus arbiter 180 in Dutton arbitrates as to

which external device takes sole control of a PCI bus. As stated in col. 4, lns. 17-36, an asserted request and acknowledge signal is provided by the bus arbiter using a unique request signal and grant signal. The arbiter in Dutton does not interpret incoming data from the local bus as received from a system bus nor arbitrate the outputting of data on the local bus from the graphics processing circuit and the audio processing circuit since no interpretation of incoming data from the local bus is necessary due to the unique request signal and grant signal. No discussion in the cited portion of Dutton make mention of any interpretation of incoming data as part of the bus arbiter and that arbiter output data on the local bus. Since the references do not teach what is alleged, Applicant respectfully submits that the claims are in condition for allowance.

In addition, Dutton actually teaches an opposite structure from that claimed and does not teach a combined video graphics and audio processing circuit but to the contrary, also requires that the video adapter 170 and audio adapter 172 be separate devices each capable of sending their own bus request signals and receive their own bus grant signals to take over the PCI bus. Accordingly, the combination of references would not teach or suggest the claimed subject matter.

As to claim 2, the claim requires that the bus arbitrator, which is alleged to be the control logic 150 in Kim, comprises an address decoder that receives an address via the local bus to route received data to the audio processing circuit when the address identifies the audio processing circuit and to route received data to the graphics processing circuit when the address identifies the graphics processing circuit. The office action cites col. 4, lns. 40-55 as allegedly teaching this subject matter. However, Applicant respectfully submits that the cited portion makes no reference to the control logic 150 routing received data from the local bus as received from the system bus to the audio processing circuit when an address decoder in the control logic

identifies the audio processing circuit and routes received data to the graphics processing circuit when the address identifies the graphics processing circuit. In fact, a different operation is described wherein a selection signal SLT is used to control the control logic to switch between graphics operation and audio operation. There is no audio address and graphics address decoding, detecting or routing occurring in the cited portion. Accordingly, Applicant respectfully submits that the claim is in condition for allowance. The other dependent claims add additional novel and non-obvious subject matter.

As to claim 6, FIG. 3 is cited as allegedly showing a method for bus arbitration between an audio processing circuit and a graphics processing circuit. However, FIG. 3 does not describe any bus arbitration scheme since the bus arbitrator and memory controller 14 is not shown in FIG. 3. FIG. 3 is the graphic and sound coprocessor 15. It is also alleged that the control logic determines whether at least one address identifies at least one of the audio processing circuit and the graphics processing circuit by stating that this is "as cited above". However, as noted above the control logic 150 does not have such an operation as it does not need such an operation since a select signal SLT is used. In addition, there is no citation found in the office action to this subject matter. Accordingly, Applicant respectfully submits that the claim is in condition for allowance. In addition, it is alleged that "it is implied that there's a chance an address in the system memory identifies both sound engine and graphics engine" (office action, page 5) referring to FIG. 2 of Kim. However, Applicant respectfully submits that there is no implication of any chance of an address in the system memory identifying both sound engine and graphics engine as alleged. A reference must teach or suggest the subject matter. Speculation is an improper basis for rejection. Also, there is no address based arbitration taught or suggested by

Kim in the cited portion. Accordingly, Applicant respectfully submits that this claim is in condition for allowance.

As to claim 14, the office action indicates that it is based on the same reasons given for claims 6 and 7. Accordingly, this claim is also in condition for allowance as noted above.

As to claim 17, Applicant respectfully reasserts the relevant remarks made above and as such, this claim is also in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter.

Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: January 22, 2010

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